



2814

PATENT

Attorney Docket No.: SAM-0219

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Jae-Phil Boo, et al.

Examiner: Pham, L.

Serial No.: 09/902,243

Group Art Unit: 2814

Filing Date: July 10, 2001

Title: METHOD OF FABRICATING A NON-VOLATILE MEMORY DEVICE
HAVING A TUNNEL-INSULATING LAYER INCLUDING MORE THAN
TWO PORTIONS OF DIFFERENT THICKNESS

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Post Office as First Class Mail on the date indicated below in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

July 22, 2003
Date

Lisa Sanders
Lisa Sanders

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following listed items:

1. Response in response to Office Action mailed on April 22, 2003; and
2. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 50-1798. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

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RESPONSE

Sir:

The following is in response to the Office Action dated April 22, 2003.

Claims 1 and 3-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the applicants' admitted prior art (AAPA) of this application in view of Liu, et al. (U.S. Patent No. 6,248,641). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicants' invention of independent claim 1 is directed to a method of fabricating a non-volatile memory device. A tunnel insulating layer, a floating gate conductive layer and a first insulating layer are formed sequentially over a semiconductor substrate. The tunnel insulating layer includes at least two portions of different thickness, and the floating gate conductive layer serves as a floating gate in a transistor device formed as part of a memory cell in the memory device. The resultant structure is etched to a given depth to form trenches, and a

second insulating layer is deposited over said structure including the trenches. The second insulating layer is selectively removed so as to form element isolation regions composed of the trenches filled with the second insulating layer. The first insulating layer is removed. The second insulating layer is selectively removed using a chemical mechanical polishing(CMP) process until a surface of the floating gate conductive layer is substantially even with a surface of the second insulating layer and the floating gate conductive layer is used as a stopping layer for the CMP process.

It is believed that the invention of independent claim 1 distinguishes the cited prior art.

The applicants maintain that the AIPA of the application does not show using a conductive floating gate layer as a stopping layer during a CMP process. Liu, et al. fail to teach or suggest using a conductive layer that serves as a floating gate of a transistor as a stopping layer during a CMP process. These features are set forth in the claims.

Specifically, referring to Liu, et al. at Figure 2F and the description at column 3, lines 10-14, a polysilicon layer 21 serves as an etch stopping layer during a CMP process. However, the polysilicon layer 21 is removed after the CMP process. As a result, the polysilicon layer 21 is not used as a floating gate in a transistor forming part of the Liu, et al. device, as set forth in the amended claims. In Liu, et al., if a transistor is to be formed after the CMP process, a new floating gate conductive layer would have to be added.

The applicants emphasized these distinctions between the invention and the cited AIPA and Liu, et al. patent in their previous Amendment, and they have not yet been addressed by the Examiner. The present Office Action makes no assertion that these features of the invention, set forth in the claims, are taught or suggested by the cited prior art.

Since neither of the AIPA and the Liu, et al. references teaches or suggests the invention set forth in the independent claim 1, no combination of the references could result in teaching or suggesting the invention. Since neither of the cited references, taken alone or in combination, teaches or suggests the invention set forth in the independent claim 1, it is believed that the independent claim 1 is allowable over the cited references. With regard to dependent claims 3-9,

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it follows that these claims should inherit allowability of the independent claim 1 from which they depend.

Therefore, reconsideration of the rejections of the claims under 35 U.S.C. § 103(a) based on the AAPA and Liu, et al. is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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